IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2827
Examiner: Luan C. THAI

In Re PATENT APPLICATION Of:

Applicant(s): Makoto TERUI, et al.

Serial No.: 09/827,246

Filed: April 6, 2001

For: SEMICONDUCTOR APPARATUS WITH DECOUPLING CAPACITOR

Docket No.: IIZ-122

AMENDMENT

November 20, 2002

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Examiner's Action mailed on August 26, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 39, please replace paragraph [0130] with the following replacement paragraph:

--The die pad 901 is expanded at every side to form bonding area 917 for power supply. The semiconductor package further includes a plate 913 of high dielectric constant material provided on the die pad 901. On the plate 913, a metal plate 919 is formed. The high dielectric constant material 913 may be ceramics, such as alumina (aluminum oxide) and titan oxide. The plate 913 may be adhered between the die pad

901 and metal plate 919. The die pad 901 is bent by about 0.1 to 0.3 mm around a chip mounting area 920 so that the inner leads 905 becomes higher in level than the chip mounting area 920. The metal plate 919 is shaped to be slightly (0.5 to 1.0 mm) smaller than the die pad 901.--

IN THE CLAIMS:

Please cancel claims 47 and 54 without prejudice or disclaimer to the subject matter recited therein.

Please amend the claims as follows:

46. (Twice Amended) A semiconductor apparatus, comprising:

a substrate;

a die pad which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the substrate and are connected to the ground terminals;

second conductive patterns which are formed on the substrate and are connected to the power supply terminals and the power supply bonding area;

a high dielectric constant layer formed on the die pad; and

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area

surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns, wherein the metal layer is provided with a ridge completely surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

50. (Amended) A semiconductor apparatus according to claim 46, wherein the ridge separates the chip mounting area from the ground bonding area.

53. (Amended) A ball grid array semiconductor package, comprising:

an substrate;

a die pad which is formed on an upper surface of the substrate, and which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the upper surface of the substrate and are connected to the ground terminals;

second conductive patterns which are formed on the upper surface of the substrate and are connected to the power supply terminals and the power supply bonding area;

a high dielectric constant layer formed on the die pad;

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area

surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns, the metal layer being provided with a ridge that completely surrounds the chip mounting area so as to define the chip mounting area and ground bonding area;

ball mounting pads disposed on a lower surface of the substrate;

interconnecting patterns which electrically couple the first and second conductive patterns to respective ones of the ball mounting pads; and

solder balls mounted on the ball mounting pads.

55. (Amended) A ball grid array semiconductor package according to claim 53, wherein the high dielectric constant layer is composed of ceramics.

56. (Amended) A ball grid array semiconductor package according to claim 55, wherein the high dielectric constant layer is alumina (aluminum oxide) and titan oxide.

57. (Amended) A ball grid array semiconductor package according to claim 53, wherein the ridge separates the chip mounting area from the ground bonding area.

58. (Amended) A ball grid array semiconductor package according to claim 53, wherein the metal layer has a shape that is smaller than a shape of the die pad.

59. (Amended) A ball grid array semiconductor package according to claim 58, wherein the metal layer partially covers the die pad, and wherein the power supply bonding area is a part of the die pad that is not covered by the metal layer.

Please add the following claim:

--62. A semiconductor apparatus, comprising:

a substrate;

a die pad formed over the substrate, said die pad having a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the substrate, in a same plane as said die pad, and are connected to the ground terminals;

second conductive patterns which are formed on the substrate, in the same plane as said die pad and said first conductive patterns, and connecting the power supply terminals to the power supply bonding area, said first conductive patterns and said second conductive patterns being formed from a common layer;

a high dielectric constant layer formed directly on the die pad without covering the power supply bonding area;

a metal layer formed directly on the high dielectric constant layer and having a chip mounting area, and a ground bonding area surrounding the chip mounting area;

a semiconductor chip mounted on the chip mounting area of said metal layer;

a first bonding wire electrically coupling the semiconductor chip to the ground bonding area, and the ground bonding area to the first conductive patterns; and

a second bonding wire electrically coupling the semiconductor chip to the power supply bonding area.--

REMARKS

The Examiner's Action mailed on August 26, 2002 has been received and its contents carefully considered.

In this Amendment, Applicants have editorially amended the specification, canceled claims 47 and 54, amended claims 46, 50, 53 and 55-59 and added claim 62. Claims 46, 48-53 and 55-62 are pending in the application. Claims 46, 53 and 62 are the independent claims. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 54-59 as being indefinite. In response thereto, various ones of these claims have been amended to correct their dependency. It is submitted that the claims pending in the application comply with all official provisions and it is requested that this rejection be withdrawn.

The Examiner has rejected claims 46, 48-49 and 51 and 52 as being obvious over *Takekawa et al.* (USP 4,714,952). Because independent claim 46 has been amended to include the subject matter from claim 47, which claim was not rejected in view of this single reference, this rejection has been rendered moot.

The Examiner has rejected claims 47 and 50 as being obvious over *Takekawa et al.* in view of *Wu et al.* Because the subject matter of claim 47 has been added into independent claim 46, Applicants will treat this rejection as applying to claim 46, as well

as to the claims dependent therefrom. It is submitted that these claims are patentably distinguishable over the cited combination of references for at least the following reasons.

Applicants' independent claim 46 has been amended to recite that a metal layer, which has a chip mounting area on which a semiconductor chip is mountable and a ground bonding area surrounding the chip mounting area, is provided with a ridge that completely surrounds the chip mounting area so as to define the chip mounting area and the ground bonding area. As disclosed by Applicants' specification, since this ridge completely surrounds the chip mounting area, conductive paste which may be used under the chip mounting area is prevented from leaking out into the bonding area. This claimed configuration is neither disclosed nor suggested by the cited references.

The Examiner's Action acknowledges that the primary reference to *Takekawa et al.* do not disclose such a ridge. The Examiner's Action relies on *Wu et al.* as disclosing this feature. However, *Wu et al.* disclose forming projecting elements 52 on opposite sides of a semiconductor 28. As is shown in Figure 5, these projecting elements 52 are disposed in two opposing rows, which extend parallel to each other, and which are arranged on opposite sides of the semiconductor 28. This reference teaches keeping the ends of the semiconductor 28 free of the projecting element 52. As such, this reference does not disclose or otherwise suggest a ridge that completely surrounds a chip mounting area as recited by Applicants' independent claim 46. Moreover, if such a configuration were utilized, for example, with the *Takekawa et al.* reference, any adhesive could still flow from the end surfaces of the semiconductor, since there would be no projecting elements disposed in this region. Applicants' claimed invention

overcomes this disadvantage. As such, it is submitted that independent claim 46, as well as the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited combination of references, and it is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner has rejected claims 53, 55, 56, 58, 59, 60 and 61 as being obvious over *Takekawa et al.* in view of *Moriyama* (USP 5,962,917). Because independent claim 53 has been amended to include the subject matter of claim 54, which claim did not form a part of this rejection, it is submitted that this rejection has been rendered moot.

The Examiner has rejected claims 54 and 57 as being obvious over *Takekawa et al.* in view of *Moriyama* and further in view of *Wu et al.* Because claim 54 has been canceled, Applicants will treat this rejection as pertaining to independent claim 53, as well as to the claims dependent therefrom. It is submitted that these claims are patentably distinguishable over the cited combination of references for at least the following reasons.

Claim 53 has been amended to recite that the metal layer is provided with a ridge that completely surrounds the chip mounting area so as to define the chip mounting area and ground bonding area. As noted above with respect to independent claim 46, none of the cited references disclose or otherwise suggest this feature. As such, it is submitted that independent claim 53, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited references, and it is requested that these claims be allowed and that this rejection be withdrawn.

Applicants have added a further independent claim 62, which recites features which are neither disclosed nor suggested by the cited references. It is requested that this claim be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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